Conner Peripherals, Inc.

Cougar Series CP30204 Intelligent Disk Drive

# **Product Manual**

00501-043 Revision B

April, 1992

3081 Zanker Road San Jose, CA 95134-2128 (408) 456-4500

#### Notice

Conner Peripherals makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Conner Peripherals shall not be liable for errors contained herein or for incidental consequential damages in connection with the furnishing, performance or use of this material.

Conner Peripherals, Inc. reserves the right to change, without notification, the specifications contained in this manual.

© Copyright Conner Peripherals, Inc. No part of this publication may be reproduced or translated into any language in any form without the written permission of Conner Peripherals, Inc.

IBM, PC/AT and PC/XT are registered trademarks of International Business Machines Corporation.

# **1.0 Introduction**

This manual describes the key features, specification summary, physical characteristics, environmental characteristics, functional description, electrical interface, recommended mounting configuration, timing requirements, host address decoding, command description, operations description, and error reporting for Conner Peripheral's Cougar model CP30204.

**Revision B** 

- 1 -

# 2.0 Key Features

The CP30204 Cougar is a high performance 3.5-inch lowprofile (1.0 inch high) 213 megabyte (formatted) disk drive with 12 ms average seek time that is designed to operate on an IBM PC/AT<sup>®</sup> or equivalent in translate mode. The drives feature fast 12 ms average seek time, low 6.7 ms average rotational latency and high shock resistance.

Because the drive contains the Task File within its control logic, it requires a simplified adapter board to operate. Conner Peripherals has developed an adapter board to be used in conjunction with the drive on an AT or equivalent system, the logic and a description of this adapter board can be found in Appendix A of this document.

- High performance rotary voice coil actuator with embedded servo system
- Auto translate feature, allowing operation as any drive type (not exceeding its capacity)
- 1,7 run length limited code
- High shock resistance
- Sealed HDA
- Automatic actuator latch against inner stop upon power down
- Microprocessor-controlled diagnostic routines that are automatically executed at start-up
- Automatic error correction and retries
- 512 byte block size

- 2 -

- Emulates IBM Task File and supports additional commands
- Up to two drives may be daisy-chained on the AT interface
- 256KB segmentable cache with LRU caching algorithm
- Redundancy on entire data path from data reception
- Single burst ECC on-the-fly

**Revision B** 

- 3 -

# **3.0 Specification Summary**

## 3.1 Capacity

	CP30204
Formatted Mbytes	212.6

# **3.2 Physical Configuration**<sup>1</sup>

	CP30204
Disk Type	Thin film
Head Type	Thin film
Actuator Type	Rotary Voice-Coil
Number of Disks	2
Data Surfaces	4
Data Heads	4
Servo	Embedded
Tracks per Surface	2,124
Track Density (TPI)	2,496 TPI
Formatted Track Capacity	25,088 bytes
Bytes per Block	512
Blocks per Drive	416,304
Sectors per Track (user):	49
Buffer Size	256KB segmentable

<sup>1</sup> The physical parameters of the drive are listed in the table. The drive's default native mode is 683 cylinders, 16 heads and 38 sectors. This drive also supports Universal Translate.

- 4 -

#### 3.3 Performance

Seek Times <sup>1</sup>	
Physical Track to Track	3.0 ms
Logical (translated) track to track	7.0 ms
Average	12.0 ms <sup>2</sup>
Maximum stroke	30.0 ms
Average Latency	6.7 ms
Rotation Speed (+0.1%)	4498 RPM
Controller Overhead	< 500 μs
Data Transfer Rate (to/from Media)	2.5 Mbyte/second
Data Transfer Rate (to/from Buffer)	8.0 Mbyte/second
Start Time(Power Up) <sup>3</sup>	
(0 RPM - 4498 RPM)	typical: 10 seconds
	maximum: 15 seconds
(0 RPM - Ready)	typical: 15 seconds
	maximum: 20 seconds
Stop Time (Power Down)	typical: 15 seconds
	maximum: 20 seconds
Start/Stop cycles	20,000 minimum
Interleave	1:1

<sup>1</sup> The timing is measured through the interface with the drive operating at nominal DC input voltages. The timing is based upon the physical parameters of the disk and may be affected by translation and/or DOS overhead at the system level.

- <sup>2</sup> The average seek time is determined by averaging the seek time for a minimum of 1000 seeks of random length over the surface of the disk.
- <sup>3</sup> These numbers assume spin recovery is not invoked. If spin recovery is invoked, the maximum could be 40 seconds. Briefly removing power can lead to spin recovery being invoked.

**Revision B** 

- 5 -

## 3.4 Read/Write

Interface	Task File
Recording Method	1 of 7 RLL code
Recording Density (ID)	44,610 bits per inch
Flux Density (ID)	34,207 flux reversals per inch

## 3.5 Power Requirements (Typical)

	+5V DC ± 5% (Typical)	+12V DC ± 10% (Typical)	Power
Read/Write Mode	440 ma	400 ma	7.0 W
Seek Mode	320 ma	420 ma	6.6 W
Idle Mode	320 ma	300 ma	5.2 W
Spin-up Mode	550 ma	1500 ma	n/a

Maximum noise allowed (DC to 1 MHZ, with equivalent resistive load):

Voltage	Noise
+5 Volt	2%
+12 Volt	1%

**Read/Write Mode** occurs when data is being read from or written to the disk.

**Seek Mode** occurs while the actuator is in motion.

**Idle Mode** occurs when the drive is not reading, writing or seeking. The motor is up to speed and DRIVE READY condition exists. Actuator is residing on last accessed track.

- 6 -

**Spin-Up Mode** occurs while the spindle motor is accelerating from its rest state to its operating speed. The specified current is the average value over the spin-up cycle.

# **3.6 Physical Characteristics**

Outline Dimensions ±.010"	1.00" x 4.00" x 5.75"
Weight	1.3 pounds

**Revision B** 

- 7 -

# 4.0 Environmental Characteristics

## 4.1 Temperature

Operating	5°C to 55°C
Non-operating	-40°C to 60°C
Thermal Gradient	20°C per hour maximum

## 4.2 Humidity

Operating	8% to 80% non-condensing
Non-operating	8% to 80% non-condensing
Maximum Wet Bulb	26°C

# 4.3 Altitude (relative to sea level)

Operating	-200 to 10,000 feet
Non-operating (maximum)	40,000 feet

# 4.4 Reliability And Maintenance

MTBF	150,000 hours (POH) <sup>1</sup>
MTTR	10 minutes typical
Preventive Maintenance	None
Component Design Life	5 years
Data Reliablity	<1 non-recoverable error in 10 <sup>13</sup> bits read

<sup>1</sup> Projected MTBF based on comparison of similar Conner products.

- 8 -

## 4.5 Shock and Vibration

Shock	1/2 sine pulse, 11 millisecond duration
Vibration	Swept sine, 1 octave per minute
Non-operating shock	75G's
Non-operating vibration	
5-62 HZ (1/2 oct/min)	0.020 inch displacement (double amplitude)
63-500 Hz (1/2 oct/min)	4 G's peak
Operating Shock	5 G's (without non-recoverable errors)
Operating Vibration 5-22 Hz 23-500 Hz	.010 inch displacement (double amplitude) .5 G's (without non-recoverable error)

## 4.6 Magnetic Field

The disk drive will meet its specified performance while operating in the presence of an externally produced magnetic field of 6 gauss DC maximum.

## 4.7 Acoustic Noise

The sound pressure level will not exceed 40 dBA at a distance of 1 meter from the drive.

Revision B

- 9 -

## 4.8 Safety Standards

Conner Peripherals disk drives are designed to comply with relevant product safety standards such as:

- UL 478, 5<sup>th</sup> edition, Standard for Information Processing and Business Equipment and UL 1950, Safety of Information Technology Equipment including Electrical Business Equipment
- CSA 22.2 #220, Information Processing and Business Equipment and CSA 22.2 #950, Safety of Information Technology Equipment including Electrical Business Equipment
- TUV-IEC 380, Safety of Electrically Energized Office Machines and TUV-IEC 950, Safety of Information Technology Equipment including Electrical Business Equipment

- 10 -

- TUV-VDE EN60950 VDE 0805/5.9
- FCC Class B Part 15 Subpart J

# 5.0 Functional Description

The drive contains all necessary mechanical and electronic parts to interpret control signals, position the recording heads over the desired track, read and write data, and provide a contaminant free environment for the heads and disks.

#### 5.1 Read/Write and Control Electronics

One integrated circuit is mounted within the sealed enclosure in close proximity to the read/write heads. Its function is to provide head selection, read preamplification, and write drive circuitry.

The dual microprocessor-controlled circuit card provides the remaining electronic functions which include:

- Read/Write Circuitry
- Rotary Actuator Control
- Interface Control
- Spin Speed Control
- Dynamic Braking

At power down the heads are automatically retracted to the inner diameter of the disk and are latched and parked on a landing zone that is off of the data tracks at the inner diameter of the disk.

#### 5.2 Drive Mechanism

A brushless DC direct drive motor rotates the spindle. The motor/spindle assembly is dynamically balanced to provide minimal mechanical runout to the disks. A dynamic brake is used to provide a fast stop to the spindle motor and return the heads to the landing zone when power is removed.

Revision B

- 11 -

### 5.3 Air Filtration System

The head-disk assembly is a sealed enclosure with an integral 0.3 micron filter which maintains a clean environment for the heads and disks.

#### 5.4 Head Positioning Mechanism

The read/write heads are supported by a mechanism coupled to a rotary voice coil actuator.

### 5.5 Read/Write Heads and Disks

Data is recorded on 95mm diameter disks through miniature 3370 type thin film heads.

#### **5.6 Customer Options**

C/D

Up to two drives may be daisy chained together utilizing the 40 pin Task File connector. The maximum cable length is 18 inches. In order to install more than one drive, it is necessary to set a jumper option. The C/D jumper is used to determine whether the drive is a master (drive C) or slave (drive D). The drive is configured as a master (drive C) when jumpered and as a slave drive (D drive) when not jumpered. (Refer to description of -PDIAG signal for further information on master/slave in Conner drives.)

- 12 -

#### DSP & SS

This pair of jumpers determines the signals on pin 39 of the interface connector.

Jumper		
DSP	SS	Action
		- spindle synchronization signal disabled on pin 39.
Х		- activity LED signal available on pin 39.
		- spindle synchronization signal enabled on pin 39.
	Х	- activity LED signal disabled from pin 39.
		- pin 39 floating.

Master/slave in ATA compatible mode uses pin 39 in a time multiplexed manner to indicate that a slave drive is present. During power-on-reset or after RESET is asserted, this line is asserted by the slave drive within 400 ms to indicate its presence. The master drive allows up to 450 msec for the slave drive to assert -HOST SLV/ACT. -HOST SLV/ACT is deasserted by the slave drive following its acceptance of the first valid command or after 31 seconds, whichever comes first.

#### Jumpers E1, E2, E3

E1	Jumper in disables spin-up at power-on. The drive will automatically spin up when it receives a command which accesses the drive.
E2	Unused
E3	Unused

Revision B

- 13 -

#### **J3 Connector**

A drive select LED may be driven using two alternative pins on this drive. Pin 39 on the interface connector can be used to drive the LED with a current limited 5 volt supply if it is not configured for Spindle Synchronization. The 16-pin auxiliary connector (J3), pins 3 and 4 provide an open collector drive signal and a current limiting resistor connected to +5V.

The spindle synchronization signal is also available on Pin 2 of J3.

- 14 -

# 6.0 Mounting Configuration

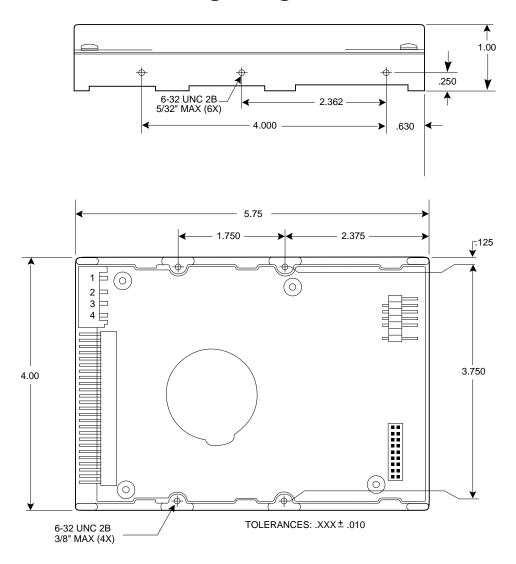


Figure 1. Mounting Configuration

**Revision B** 

- 15 -

### 7.1 Seek Times

The timing is measured through the interface with the drive operating at nominal DC input voltages. The timing also assumes that the BIOS and PC system hardware dependency have been subtracted from timing requirements and that the drive is operated using its native drive parameters.

Average seek time is determined by averaging the seek time for a minimum of 1000 seeks of random length over the disk surface.

#### 7.2 Start Time (Power Up)

Numbers specified assume that spin recovery is not invoked. If spin recovery is invoked, the max could be 40 seconds. Briefly removing power can lead to spin recovery being invoked.

#### 7.3 Shock

Drives are subjected to specified G level shock for 11 milliseconds with a 1/2 sine wave pulse. The drive meets specification without suffering non-recoverable READ or WRITE errors or other damage.

#### 7.4 Vibration

Drives are subjected to specified vibration levels at 1/2 octave per minute sweep. The drive meets the specification without non-recoverable errors, READ or WRITE errors, or other damage.

- 16 -

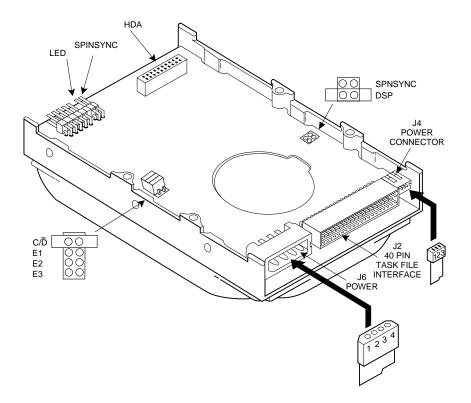


Figure 2. Connectors and Jumper Options

**Revision B** 

- 17 -

#### **8.1 Power Connectors**

The drive has two power connectors; a standard 4 pin DC power connector and a smaller 3 pin connector. Power must only be supplied at one source.

The mating connector for the 4 pin connector is AMP 1-480424-0 (Housing) and AMP 60619-4 (loose piece) or 61117-4 (strip) contacts.

The following table describes the 4 pin power connector pins:

Pin	Signal
1	+12V
2	GND
3	GND
4	+5V

The mating connector for the three pin connector is Molex series 54-84 Header, housing Molex part number 39-01-0033 and terminal part number 39-00-0031 (loose) or 39-00-0023 (strip).

The following table describes the 3 pin power connector pins.

Pin	Signal
1	+5V
2	+12V
3	GND

- 18 -

# 9.0 Host Interface

#### 9.1 Description

The interface between the drive adapter and the drive is called the Host Interface. The set of registers in I/O space of the Host controlled through the Host Interface is known as the Task File. The physical interface from the drive to the host is implemented using a 40 pin connector.

#### 9.2 Interface Connector

The recommended mating connector is Molex P/N 15-47-3401 or equivalent. Two drives may be daisy chained on this connector, and the maximum cable length is 18 inches.

#### 9.3 Signal Levels

All signal levels are TTL compatible. A logic 1 is > 2.0 Volts. A logic 0 is from 0.00 Volts to .70 Volts.

#### 9.4 Signal Conventions

All signals on the Host Interface shall have the prefix HOST. All active low signals shall be further prefixed with a "-" designation. All active high signals shall be prefixed with a '+' designation. Signals driven only by the Host will be indicated with an O, the signals driven by the drive with an I, and signals which can be driven by either the Host or the drive will be indicated with an I/O.

**Revision B** 

- 19 -

# 9.5 Pin Descriptions

The following table describes all of the pins on the Task File Interface.

Pin	Signal	Pin	Signal
01	-HOST RESET	02	GND
03	+HOST DATA 7	04	+HOST DATA 8
05	+HOST DATA 6	06	+HOST DATA 9
07	+HOST DATA 5	08	+HOST DATA 10
09	+HOST DATA 4	10	+HOST DATA 11
11	+HOST DATA 3	12	+HOST DATA 12
13	+HOST DATA 2	14	+HOST DATA 13
15	+HOST DATA 1	16	+HOST DATA 14
17	+HOST DATA 0	18	+HOST DATA 15
19	GND	20	KEY
21	RESERVED	22	GND
23	-HOST IOW	24	GND
25	-HOST IOR	26	GND
27	RESERVED	28	+HOST ALE
29	RESERVED	30	GND
31	+HOST IRQ14	32	-HOST IO16
33	+HOST ADDR 1	34	-HOST PDIAG
35	+HOST ADDR 0	36	+HOST ADDR 2
37	-CS0	38	-CS1
39	-HOST SLV/ACT	40	GND

- 20 -

Signal Name	Dir	Pin	Description
-HOST RESET	0	1	Reset signal from the Host system which is active low during power up and inactive thereafter.
GND	0	2	Ground between the drive and the Host.
+HOST DATA	I/O	3-18	16 bit bi-directional data bus 0- 15 between the host and the drive. The lower 8 bits, HD0- HD7, are used for register & ECC access. All 16 bits are used for data transfers. These are tri-state lines with 24 mA drive capability.
GND	0	19	Ground between the drive and the Host.
KEY	N/C	20	An unused pin clipped on the drive and plugged on the cable. Used to guarantee correct orientation of the cable.
RESERVED	0	21,27,	29
GND	0	22	Ground between the drive and the host.
-HOST IOW	0	23	Write strobe, the rising edge of which clocks data from the host data bus, HD0 through HD15, into a Task File register on the drive.
GND	0	24	Ground between the drive and the host.

**Revision B** 

- 21 -

Signal Name	Dir	Pin	Description
-HOST READ IOR	Ο	25	Read strobe, which when low enables data from Task File on the drive onto the host data bus, HD0 through HD15. The rising edge of -HOST IOR latches data from the drive at the host.
GND	0	26	Ground between the drive and the Host.
+HOST ALE	0	28	Host Address Latch Enable. A signal used to qualify the address lines. This signal is presently not used .
GND	0	30	Ground between drive and host.
+HOST IRQ14	I	31	Interrupt to the Host system, enabled only when the drive is selected, and the host activates the -IEN bit in the Digital Output register. When the -IEN bit is inactive, or the drive is not selected, this output is in a high impedance state, regardless of the state of the IRQ bit. The interrupt is set when the IRQ bit is set by the drive CPU. IRQ is reset to zero by a Host read of the Status register or a write to the Command register. This signal is a tri-state line with 8 ma drive capacity.

- 22 -

Signal Name	Dir	Pin	Description
-HOST IO16	I	32	Indication to the Host system that the 16 bit data register has been addressed and that the drive is prepared to send or receive a 16 bit data word. This line is tri-state line with 24 mA drive capacity.
-HOST PDIAG	I	34	Passed diagnostic. At POR, PDIAG will be activated by the slave within 1 ms. If the master doesn't see -PDIAG active after 4 ms it will assume no slave is presentPDIAG will remain active until the slave is ready to go not busy or 14.0 seconds on a power on reset. The master will wait 14.5 seconds or until the slave deactivates -PDIAG on power on reset before it goes not busy. The slave will de- activate -PDIAG and go not busy, if it is not ready after the 14.0 seconds. Neither drive will set ready or seek complete until they have reached full spin speed and are ready to read/write.

**Revision B** 

- 23 -

Signal Name	Dir	Pin	Description
			During a software reset, -PDIAG will be activated by the slave within 1 ms. If the master doesn't see -PDIAG active after 4 ms it will assume no slave is present. The slave will not de- activate -PDIAG until it is ready to go not busy or 400 ms. The master will only wait 450 milliseconds or until the slave deactivates -PDIAG before wait 450 milliseconds before it activates -PDIAG and goes not busy. The slave will not set ready or seek complete until those states are achieved.
			After reset, -PDIAG will be used for the diagnostic command in the following manner. It is output by the drive if it is the slave drive, input to the drive if it is the master drive. This low true signal indicates to a master that the slave has passed its internal diagnostic command. This line is only inactive high during execution of the diagnostic command.
+HOST A0,A1,A2	0	35 33,36	Binary coded address used to select the individual registers in the Task File.

- 24 -

Signal Name	Dir	Pin	Description
-HOST CS0	0	37	Chip select decoded from the host address bus. Used to select some of the Host accessible registers. NOTE: This signal should be disabled by the Host when data transfers are in progress.
-HOST CS1	0	38	Chip select decoded from the Host address bus. Used to select three of the registers in the Task File.
-HOST SLV/ACT	I	39	Signal from the drive used either to drive an activity LED or as a signal for synchronizing spindles of a drive array, or as an indication of a second drive present. (See the Customer Options section for further information).
GND	0	40	Ground between the drive and the host.

**Revision B** 

- 25 -

# 9.6 Auxiliary Connector

The Auxiliary connector is used to provide optional signals at the front of the drive. No connection should be made to the pins marked RESERVED. These pins are reserved for factory test purposes and improper connection may adversely affect the drive.

Pin	Signal	Pin	Signal
01	GND	02	Spindle Sync
03	+LED	04	-LED
05	KEY	06	KEY
07	RESERVED	08	RESERVED
09	RESERVED	10	RESERVED
11	RESERVED	12	RESERVED
13	RESERVED	14	RESERVED
15	RESERVED	16	RESERVED

- 26 -

## 10.1 Host Programmed I/O 8/16 Bit Timing Parameters

The values in the table below refer to the timing diagram in Figure 3.

<b>Symbol</b> RDS	Parameter IOR low to HD[0:15]	Min	<b>Max</b> 60	<b>Units</b> ns
RDHLD	IOR high to HD[0:15]	5	00	ns
WDS	HD[0:15] setup to IOW high	20		ns
WDHLD RWPULSE	HD[0:15] hold from IOW high IOR*/IOW pulse width	10 75		ns ns
ADRSET	HCSO, A0:2, A9/HCS1 setup to IOR*/IOW* low	15		ns
ADRHLD	Address hold from IOR/IOW high	10	75	ns
RWA	IOR* High to IOR* Low	50		ns
CS16L	A0:2, HCSO setup to IOCS16* active		30	ns
IOCS16HLD	IO16 hold time		70	ns

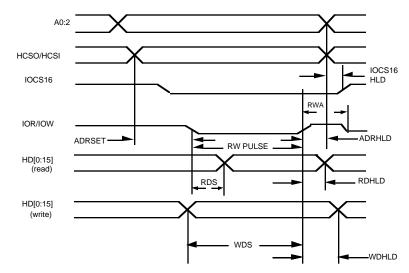


Figure 3. Timing Diagram

**Revision B** 

- 27 -

# 10.2 Host DMA 8/16 Bit Interface Timing Parameters

The values in the table below refer to the timing diagram in Figure 4.

Symbol	Parameter	Min	Мах	Unit
DREQL	DREQ low from DACK low		40	ns
RDS	IOR low to HD[0:15] valid		60	ns
RDHLD	IOR high to HD[0:15] tri-state	5		ns
WDS	HD[0:15] setup to IOW high	20		ns
RWPULSE	IOR/IOW pulse width	75		ns
DACKS	Dack low to IOR low	0		ns
DACKH	Dack hold from IOR high	0		ns
RWA	IOR low to IOR high	50		ns
BDS	Between Sector Delay	270		ns
WDHLD	Write data Hold from IOW* High	10		ns

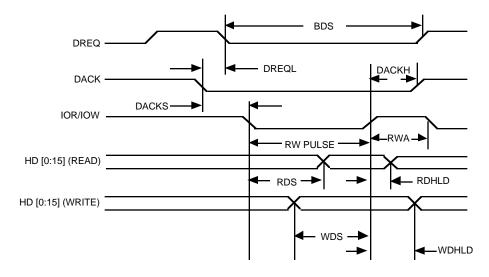


Figure 4. Timing Diagram

- 28 -

## **11.0 Host Address Decoding**

The Host addresses the drive using programmed I/O. This method requires that the desired register address be placed on the three Host address lines (HA2-HA0), a proper CHIP SELECT is asserted and a READ or WRITE strobe (-HOST IOR/-HOST IOW) is then sent to the drive.

The Host generates one of two independent chip selects on the interface. The high order chip select, -HOST CS1, is used to access register 3F6 or 3F7. The low order chip select, -HOST CS0, is used to address registers 1F0 - 1F7. The ECC bytes are transferred on bits 7-0.

The Host data bus 15-8 is only enabled when IO16 Enable is active and the Host is addressing the data register for transferring data, and are only transferred if the operation is a READ or WRITE LONG.

**Revision B** 

- 29 -

The following I/O map defines all of the register addresses and functions for these I/O locations. A description of each register follows.

Addr <sup>1</sup>	-CS0	-CS1	HA	HA	HA	Read Function	Write Function
			2	1	0		
	1	1	х	х	х	No operation	No Operation
	0	0	х	х	х	Invalid address	Invalid address
	1	0	0	х	х	High Impedance	Not used
	1	0	1	0	х	High Impedance	Not used
1F0	0	1	0	0	0	Data Register	Data Register
1F1	0	1	0	0	1	Error Register	Write Precomp Reg.
1F2	0	1	0	1	0	Sector Count	Sector Count
1F3	0	1	0	1	1	Sector Number	Sector Number
1F4	0	1	1	0	0	Cylinder Low	Cylinder Low
1F5	0	1	1	0	1	Cylinder High	Cylinder High
1F6	0	1	1	1	0	SDH Register	SDH Register
1F7	0	1	1	1	1	Status Register	Command Reg.
3F6	1	0	1	1	0	Alternate Status Reg.	Digital Output Reg.
3F7	1	0	1	1	1	Drive Address Reg.	Not used

x=don't care

<sup>1</sup> These I/O port addresses are listed for programmer reference. They are a function of I/O decoding in the Host Adapter, such as the Conner AT Adapter Card shown in Appendix A. These I/O addresses are required for compatibility with typical AT BIOS.

- 30 -

### **11.1 Register Description**

In the following register descriptions, unused write bits should be written with zeros and unused read bits should be read as zeroes.

#### 11.2 Data Register (-HOST CS0, address 0, R/W)

The data register is the register through which all data is passed on READ and WRITE commands. It is also the register to which the sector table is transferred during FORMAT commands and the register data associated with the IDENTIFY command is transferred. All transfers are 16 bit I/O operations, except for ECC bytes transferred during R/W LONG commands. ECC transfers 8 bit operations that occur after the transfer of the data.

Data is stored on the disk with the Least Significant Byte first, then the Most Significant Byte for each word. This is important to remember when testing the ECC circuitry.

**Revision B** 

- 31 -

#### 11.3 Error Register (-HOST CS0, address 1, read only)

The Error Register contains status from the last command executed by the drive. The contents of this register are only valid when the error bit (ERR) is set in the Status Register, unless the drive has just powered up or completed execution of its internal diagnostic, in which case the register contains a status code. The error bits in the register are defined below. The status codes are discussed later in the description of the DIAGNOSTIC Command.

b7	b6	b5	b4	b3	b2	b1	b0
BBK	UNC		IDNF		ABRT	тко	

where:

**BBK** indicates that a bad block mark was detected in the requested sector's ID field. A bad block mark is not created in the factory, but only when requested in the format command.

**UNC** indicates that a non-correctable data error has been encountered.

**IDNF** indicates that the requested sector's ID field could not be found.

**ABRT** indicates that the requested command has been aborted due to a drive status error (not ready, write fault, etc.) or because the command code is invalid.

**TK0** indicates that track 0 has not been found during a recalibrate command.

-- not used. These bits are set to zero.

- 32 -

For other drives b0 is AMNF (Address Mark Not Found.) This is not used on Conner drives.

#### 11.4 Write Precomp Register (-HOST CS0, address 1 write only)

This register was previously used to set write precompensation in non-intelligent disk drives. This drive uses the Write Precomp Register for Commands EF and Fx.

#### 11.5 Sector Count (-HOST CSO, address 2, R/W)

The Sector Count defines the number of sectors of data to be read or written. If the value in this register is zero, a count of 256 sectors is specified. This count is decremented as each sector is read such that the register contains the number of sectors left to access in the event of an error in a multi-sector operation.

In addition, the contents of this register define other parameters in non-read/write commands as follows:

- This register is used to specify the number of sectors per track when executing an INITIALIZE DRIVE PARAMETERS command.
- This register is used in the POWER commands to provide the power down time-out parameter and status.
- This register is used to specify the number of sectors per block in the SET MULTIPLE command.

**Revision B** 

- 33 -

#### 11.6 Sector Number (-HOST CS0, address 3, R/W)

This register contains the starting sector number for any disk access. At the completion of each sector, and at the end of the command this register is updated to reflect the last sector read correctly, or the sector on which an error occurred. During multiple sector transfers, this register is updated to point at the next sector to be read/written if the previous sector's operation was successful.

- 34 -

## 11.7 Cylinder Low (-HOST CS0, address 4, R/W)

The Cylinder Low Register contains the low order 8 bits of the starting cylinder number for any disk access. At the completion of each sector, and at the end of the command, this register is updated to reflect the current cylinder number.

## 11.8 Cylinder High (-HOST CS0, address 5, R/W)

The Cylinder High Register contains the two high order bits of the starting cylinder number for any disk access. At the completion of each sector, and at the end of the command, this register is updated to reflect the current cylinder number.

Revision B

- 35 -

#### 11.9 SDH Register (-HOST CS0, address 6, R/W)

This register contains the drive and head numbers, as defined below:

b7	b6	b5	b4	b3	b2	b1	b0
Don't	0	Don't	DRV		HE	AD	
care		care					

where:

**DRV** is the binary encoded drive select number. When this bit is reset, the master drive is selected, and when this bit is set, the slave drive is selected. While the Task File Registers in the Master and Slave drives are simultaneously written, this bit selects which drive will respond to and execute the command.

**HEAD** is the four bit binary encoded head select number.

At the completion of each sector, and at the end of the command, this register is updated to reflect the currently selected head.

- 36 -

## 11.10 Status Register (-HOST CS0, address 7 read only)

This register contains the drive/controller status. The contents of this register are updated at the completion of each command. If the BSY bit is active, no other bits are valid. The Host reading this register when an interrupt is pending is considered to be the interrupt acknowledge. Any pending interrupt is cleared when this register is read.

The bits in this register are defined below:

	b7	b6	b5	b4	b3	b2	b1	b0
ſ	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

where:

**BSY** is the busy bit, which is set when the drive is accessing to the Task File registers and the Host is locked out from accessing the Task File. This bit is set under the following circumstances:

- 1) At activation of the HOST RESET pin in the interface, or at activation of the software reset bit in the digital output register.
- 2) Immediately upon Host write of the command register with a Read, Read Long, Read Buffer, Seek, Recalibrate, Initialize Drive Parameters, Read Verify,Identify, or Execute Drive Diagnostic command.

**Revision B** 

- 37 -

3) Immediately following transfer of: A) 512 bytes of data after Host write of the command register with a Write, Format Track, or Write Buffer command, or B) 512 bytes of data and the ECC bytes after a Host write of the Command register with a Write Long command. When BSY is active, any Host read of a Task File register is inhibited and the Status register is read instead.

**DRDY** is the drive ready indication. When there is an error, this bit is not changed until the Status register is read by the Host, at which time the bit again indicates the current readiness of the drive. This bit will be reset at power up and remain reset until the drive is up to speed and ready to accept a command.

**DWF** is the drive write fault bit. When there is an error, this bit is not changed until the Status register is read by the Host, at which time the bit again indicates the current write fault status.

**DSC** is the drive seek complete bit. It is an indication that the actuator is on track. When there is an error, this bit is not changed until the Status register is read by the Host, at which time the bit again indicates the current readiness of the drive. This bit will be reset at power up and will remain reset until the drive is up to speed and ready to accept a command.

**DRQ** is the data request bit, which indicates that the drive is ready for transfer of a word or a byte of data between the Host and the Data register.

- 38 -

**CORR** is the corrected data bit, which is set when a correctable data error has been encountered and the data has been corrected and on a read verify if any sector was corrected the bit is valid. This condition will not terminate either a MULTI-SECTOR READ or a READ MULTIPLE command.

**IDX** is the index bit which is set once per disk revolution.

**ERR** is the error bit, which indicates that the previous command ended in some type of error. The other bits in the Status register, and the bits in the error register will have additional information as to the cause of the error.

## 11.11 Alternate Status Register (-CS1, address 6, read only)

This register contains the same information as the Status register in the Task File. The only difference being that reading this register does not imply interrupt acknowledge to reset a pending interrupt.

b7	b6	b5	b4	b3	b2	b1	b0
BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

See the description of the Status register for definitions of the bits in this register.

## 11.12 Digital Output Register (-CS1, address 6, write only)

This register contains two control bits as follows:

b7	b6	b5	b4	b3	b2	b1	b0
					SRST	-IEN	

Revision **B** 

- 39 -

where:

**-IEN** is the enable bit for this disk drive interrupt to the Host. When this bit is active, and the drive is selected, the Host interrupt, +IRQ, is enabled, through a tri-state buffer, to the Host. When this bit is inactive, or the drive is not selected the +IRQ pin will be in a high impedance state, regardless of the presence or absence of a pending interrupt.

**SRST** is the Host software reset bit. The drive is held reset when this bit is active, and enabled when this bit is inactive.

-- these bits are not used.

### 11.13 Drive Address Register (-CS1, address 7, read only)

This register loops back the drive select and head select addresses of the currently selected drive. The bits in this register are as follows:

b7	b6	b5	b4	b3	b2	b1	b0
RSVD	-WTG	-HS3	-HS2	-HS1	-HS0	-DS1	-DS0

where:

**RSVD** is reserved and not driven by the drive. When the Host reads the drive address register, this bit must be in a high impedance state.

**-WTG** is the write gate bit, which is active when writing to the disk drive is in progress.

- 40 -

-**HS3 through** -**HS0** are the one's complement of the binary coded address of the currently selected head. For example, if -HS3 through -HS0 are 1 1 0 0, respectively, head 3 is selected.

-**DS1** is the drive select bit for drive 1, and should be active when drive 1 is selected and active. -DS0 is the drive select bit for drive 0, and should be active when drive 0 is selected and active. It is important to note that Bit 7 is not driven for compatibility with the floppy drive address space. If your system is different, you may have to drive this bit when this register is read.

Revision B

- 41 -

# **12.0 Command Description**

All commands are decoded from the Command Register. The Host interface shall be programmed by the Host computer to perform commands and will return status to the Host at command completion. When two drives are daisy chained on the interface, commands are written in parallel to both drives, only the selected drive will execute the command, except for the diagnostic command. In that case, both drives execute the command and the slave drive reports its status to the master via the -HOST PDIAG signal.

Drives are selected by the DRV bit in the drive/head Register and by a jumper, on the drive designating it as either a master or slave. When the DRV bit is set to 0, the master drive (C) is selected, and when the DRV bit is set to 1, the slave drive (D) is selected. When drives are daisy chained, one must be jumpered as the master and one as the slave. When a single drive is attached to the interface, it must be jumpered as the master. Throughout this document, drive selection always refers to the state of the DRV bit, and position of the master/slave jumper.

To issue a command, load the pertinent registers in the Task File, activate the interrupt enable bit, -IEN in the Digital Output Register, and then write the command code to the Command Register. Execution begins as soon as the Command Register is written.

Also see the section on retries.

- 42 -

Command Name Used		(	Com	man	d Co	ode			Ра	ramet	ers		
	b7	b6	b5	b4	b3	b2	b1	b0	SC	SN	CY	SDH	PR
Recalibrate	0	0	0	1	х	х	х	х	n	n	n	d	n
Read Sector(s)	0	0	1	0	0	0	L	r	У	У	У	у	n
Write Sector(s)	0	0	1	1	0	0	L	r	У	У	У	у	n
Read Verify Sector(s)	0	1	0	0	0	0	0	r	У	У	У	у	n
Format Track	0	1	0	1	0	0	0	0	n	n	У	у	n
Seek	0	1	1	1	х	Х	х	х	n	n	У	у	n
Execute Drive Diag.	1	0	0	1	0	0	0	0	n	n	n	d	n
Initialize Drive Parms	1	0	0	1	0	0	0	1	У	n	n	у	n
Read Multiple	1	1	0	0	0	1	0	0	У	У	У	у	n
Write Multiple	1	1	0	0	0	1	0	1	У	У	У	у	n
Set Multiple Mode	1	1	0	0	0	1	1	0	У	n	n	d	n
Power Commands	1	1	1	0	р	р	р	р	У	n	n	d	n
Read Sector Buffer	1	1	1	0	0	1	0	0	n	n	n	d	n
Write Sector Buffer	1	1	1	0	1	0	0	0	n	n	n	d	n
Identify Drive	1	1	1	0	1	1	0	0	n	n	n	d	n
Set Look Ahead	1	1	1	0	1	1	1	1	n	n	n	d	у
Translate Command	1	1	1	1	0	0	0	1	n	У	У	у	у
Physical Seek	1	1	1	1	0	0	1	0	n	n	У	у	у
Defect List	1	1	1	1	0	1	0	1	n	У	n	d	у
Enable Index	1	1	1	1	0	1	1	0	n	n	n	d	у

where:

L is the long bit, if 1, r/w long commands are executed, if 0, normal r/w commands are performed.

**Revision B** 

- 43 -

**r** is the retry bit; 0 = retries are enabled, 1 = retries are disabled. Retries that may be enabled/disabled are those on ECC and data errors. When retries are disabled at the start of a command, they are always automatically enabled at the end of the command.

**SC** is the sector count register.

**SN** is the sector number register.

**CY** is the cylinder registers.

**SDH** is the drive/head register.

**PR** is the write precomp register.

**y** means the register contains a valid parameter for this command. For the drive/head register, Y means that both the drive and head parameters are used.

**n** means the register does not contain a valid parameter for this command.

**d** means only the drive parameter is valid and not the head parameter.

**p** is a valid bit for power commands EO-E3 and E5-E6.

 $\mathbf{x} = \mathbf{don't} \mathbf{care}.$ 

- 44 -

# 12.1 Recalibrate - 10

This command will move the R/W heads from anywhere on the disk to cylinder 0. Upon receipt of the command, the drive sets BSY, resets DSC, and executes a SEEK to cylinder zero. The drive then waits for the SEEK to complete before updating status, resetting BSY, setting DSC, and generating an interrupt. If the drive cannot reach cylinder 0, the Error Bit (ERR) is set in the Status Register and the track 0 (TK0) bit set in the Error Register. An aborted command (ABRT) response will be given in the Error Register if the drive is not spinning or is not on track. Upon successful completion of the command, the Task File Registers will be as follows:

Register	Value
Error Register	00
Sector Count	Unchanged
Sector Number	Unchanged
Cylinder Low	00
Cylinder High	00
SDH	Unchanged

Revision B

- 45 -

## 12.2 Read Sector(s) - 2X

This command will read from 1 to 256 sectors as specified in the Task File (sector count equal to 0 requests 256 sectors), beginning at the specified sector. As soon as the Command Register is written, the drive sets the BSY bit and begins execution of the command.

The Error bit (ERR) is set in the Status Register and the Error Register is updated; (1) if bits 2 & 3 are not equal to zero, then the Aborted Command bit (ABRT) is set, (2) if incorrect Task File parameters are passed, the ID Not Found Error (IDNF) is set.

If the drive is not already on the desired track, an implied SEEK is performed. Once at the desired track, the drive begins searching for the appropriate ID field. If the ID is read correctly, the data field is read into the sector buffer, Error Bits are set if an error was encountered, the DRQ bit is set and an interrupt is generated. The DRQ bit is always set regardless of presence or absence of an error condition at the end of the sector. Upon command completion, the Task File Registers contain the cylinder, head, and sector number of the last sector read. The sector count is zero after successful execution of the command.

Multiple sector reads set DRQ and generates an interrupt when the sector buffer is filled at the completion of each sector, and the drive is ready for the data to be transferred to the Host. DRQ is reset and BSY is set immediately after the Host empties the sector buffer.

- 46 -

If an error occurs during a multiple sector read, the read will terminate at the sector where the error occurs. The Task File Registers will contain the cylinder, head, and sector number of the sector where the error occurs. The Host may then read the Task File to determine what error has occurred, and on which sector. If the error was either a Correctable Data Error or an Non-correctable Data Error, the flawed data is loaded into the sector buffer. The read does not terminate if the error was a Correctable Data Error.

If no error is detected, the cylinder, head, and sector Registers are updated to point to the next sequential sector.

A read long may be executed by setting the long bit in command code. The read long command returns the data and the ECC bytes contained in the data field of the desired sector. During a read long, the drive does not check the ECC bytes to determine there has been any type of data Error. Data bytes are 16 bit transfers and ECC bytes are 8 bit transfers.

## 12.3 Write Sector(s) - 3X

This command will write from 1 to 256 sectors as specified in the Task File (sector count equal to 0 requests 256 sectors), beginning at the specified sector. As soon as the Command Register is written, the drive waits for the Host to fill the sector buffer with the data to be written. No interrupt is generated to start the first buffer fill operation. Once the buffer is full, the drive sets BSY and begins command execution.

**Revision B** 

- 47 -

The Error bit (ERR) is set in the Status Register and the Error Register is updated, (1) if bits 2 & 3 are not equal to zero, (then the Aborted Command bit, ABRT, is set), or (2) if incorrect Task File parameters are passed, the ID Not Found Error, IDNF, is set.

If the drive is not already on the desired track, an implied SEEK is performed. Once at the desired track, the drive begins searching for the appropriate ID field. If the ID is correct, the data loaded in the buffer is written to the data field of the sector, followed by the ECC bytes. Upon command completion, the Task File Registers contain the cylinder, head, and sector number of the last sector written. The sector count is zero after successful execution of the command.

Multiple sector writes set DRQ and generate an interrupt each time the buffer is ready to be filled. DRQ is reset and BSY is set immediately when the Host fills the sector buffer. If an Error occurs during a multiple sector write, it will terminate at the sector where the error occurs. The Task File indicates the location of the sector where the error occurred. The Host may then read the Task File to determine what error has occurred, and on which sector. If no error is detected, the cylinder, head, and sector Registers are updated to point at the next sequential sector.

A write long may be executed by setting the long bit in the command code. The write long command writes the data and the ECC bytes directly from the sector buffer; the drive will not generate the ECC bytes itself for the write long command. Data byte transfers are 16 bits, ECC bytes are 8 bit transfers.

- 48 -

# 12.4 Verify Sectors - 4X

This command functions similarly to the READ SECTORS command except that no data is transferred to the host and at completion of the command the CORR bit is set if software ECC correction was required. The drive remains BUSY until all data is verified. If LOOK AHEAD's are active, the VERIFY command will also work the same as when a READ is performed.

## 12.5 Format Track - 5X

The purpose of the FORMAT TRACK command is to provide a means by which a defective sector may either be marked bad or reassigned. This command has been used on other drives to do the low level formatting job of putting the header and creating the data fields for all tracks on the drive. It is not necessary to execute a FORMAT command prior to operating the drive on the Host PC because the drive is a hard sectored drive and all required low level formatting is done during the factory certification of the drive. Conner supports the FORMAT command only to allow any sectors that become defective to be handled in a fashion required by different operating systems. The FORMAT command operates on one single logical track at a time and all sectors on that track are filled with zeroes.

As indicated above, there are two methods provided to handle defective sectors. When a sector is marked bad, the ID field of the sector is updated to indicate a bad block. Any time that sector is accessed thereafter, the drive will return bad block status in the Error Register. The second method, Assign, allows a spare sector on the drive to be used to replace the specified sector. Following this operation, the drive performance will be degraded slightly when the sector is accessed due to the drive automatically going to the new sector.

**Revision B** 

- 49 -

It is also possible to format a bad block good and unassign an alternate. When a sector is un-assigned, the spare sector that was used as the alternate can be reclaimed. However, since the assigned sector could be an alternate itself it is not correct to write a diagnostic that assigns and then unassigns alternates on a large scale, because the spare sectors will be lost.

The command is similar to a write command, where the Task File parameters are written, the Command Register is written to begin the command, and the drive responds by activating DRQ in the Status Register. This indicates a request for 1 sector (512 bytes) of data that is used to describe the operations to be performed on each sector of the track specified by the Task File. After the data is written to the Data Register, the drive analyzes the information for each sector and performs the requested action to each sector. When the command is complete, the drive raises Interrupt Request with ending status in the Task File.

The data in the sector buffer must conform to a specified format. There must be one word, 2 bytes, for each sector. The words must be contiguous and begin at the start of the sector. Unlike some drives where the order of the words is used to determine the interleave, the order of the words is not significant because the drive's interleave cannot be changed. The most significant byte of each word must contain the sector number. The least significant byte must contain a descriptor byte that indicates what is to be done to each sector. There are four possible descriptor bytes:

- 1.  $00_{\rm H}$  = format sector good
- 2.  $80_{\rm H}$  = format sector bad
- 3.  $40_{\rm H}$  = assign this sector to an alternate location

- 50 -

4.  $20_H$  = unassign the alternate location for this sector

The drive will return an ID not found under the following conditions:

- 1. If there is a missing word for any sector along the track.
- 2. If the words are not contiguous from the start of the sector.
- 3. If there is more than one (1) word per sector.
- 4. If the Task File calls for an illegal cylinder and/or head Register.

A utility program to handle defective sectors should provide some interface to identify defective sectors. The program should build a 512 byte block with a word for each sector for the track containing the defective sector. The most significant byte of each word should contain the sector number. The defective sectors descriptor byte should be set to either  $80_{\rm H}$  or  $40_{\rm H}$  depending on whether or not the sector is to be formatted bad or reassigned. All of the remaining sectors should have a descriptor byte of  $00_{\rm H}$ . Once the data block is created, the FORMAT command can be executed.

It is important to remember that all data on the track is lost. The drive formats logical track as defined by the power-on-reset default, or by the values issued by the last INITIALIZE DRIVE PARAMETERS command.

**Revision B** 

- 51 -

### 12.6 Seek - 7X

This command selects the head specified in the Task File and initiates a SEEK to the desired track. When the command is issued, the drive sets BSY in the Status Register, resets SEEK COMPLETE (DSC), initiates the SEEK, resets BSY, and generates an interrupt. Only the Cylinder Register and Drive Head Register are valid for this command.

The drive does not wait for the SEEK to complete before returning the interrupt. SEEK COMPLETE (DSC) will be set upon completion of the command. If a new command is issued to a drive while a SEEK is being executed, the drive will wait, with BSY active, for the SEEK to complete before executing the new command. No checks are made on the validity of the Sector number in the Task File. The Error Bit (ERR) in the Status Register and the ID Not Found (IDNF) bit in the Error Register of the Task File will be set if an illegal cylinder number is passed.

- 52 -

## 12.7 Execute Drive Diagnostic - 90

This command performs the internal diagnostic tests implemented by the drive. The diagnostic tests are only executed upon receipt of this command. The drive sets BSY immediately upon receipt of the command. If the drive is a master, the drive performs the diagnostic tests and saves the results. It then checks to see if a slave drive is present and waits up to 5 seconds for the slave to complete its diagnostics. If the slave successfully completes its diagnostics, it asserts -HOST PDIAG. If unsuccessful, the master drive resets BSY in the Status Register, and generates an interrupt. The Error bit (ERR) is set in the Status Register and the Error Register is updated.

The value in the Error Register should be viewed as a unique 8 bit code and not as the single bit flags defined previously. The interface Registers are set to initial values except for the Error Register.

**Revision B** 

- 53 -

The table below details the codes in the Error Register and a corresponding explanation:

Error	
code	Description
01	no error detected
02	format device error
03	sector buffer error
8x	slave drive failed (see note below)

Additional codes may be implemented at the manufacturer's option.

NOTE: If the slave drive fails diagnostics, the master drive shall "OR"  $80_H$  with its own status and load that code into the Error Register. If the slave drive passes diagnostics or there is no slave drive connected, the master drive shall set bit 7 of the Error Register in the Task File to 0.

- 54 -

# 12.8 Initialize Drive Parameters - 91

This command enables the host to set the head switch and cylinder increment points for multiple sector operations. The sector count and SDH registers are used to specify the logical sectors per track and number of heads for the drive. The cylinder count is calculated by the drive based on these two parameters. In the TRANSLATE mode, the logical head and sector numbers in the Task File will be translated to their native physical values as part of execution of the command. The sector and head, values in the Task File are not checked for validity by this command. Upon receipt of this command, the drive sets BSY, saves the parameters, resets BSY, and generates an interrupt.

The UNIVERSAL TRANSLATE MODE enables the user to configure the drive to any cylinder, head, and sector configuration desired. The translate configuration is limited only by the maximum capacity of the drive. Upon initial power up of the drive it will default to a predetermined configuration detailed in the specification summary of this manual.

After the drive is ready, the host system may issue INIT DRIVE PARMS COMMAND to alter the translate configuration (number of heads and number of sectors per track). The drive parameters will then be saved in EEPROM for subsequent drive operations.

**Revision B** 

- 55 -

## 12.9 Read Multiple Command - C4

The READ MULTIPLE command is identical to the READ SECTORS operation except several sectors are transferred to the Host as a block without intervening interrupts. In addition the DRQ qualification of the transfer is required only on the first sector of the block of sectors to be transferred. Long transfers are not permitted. The block count, which is the number of sectors to be transferred as block, is programmed by the SET MULTIPLE mode command which must be executed prior to the READ MULTIPLE command. When the READ MULTIPLE command is issued, the Sector Count Register will contain the number of sectors (not the number of blocks or the block count) requested.

If this sector count is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer will be for N sectors, where

N = (sector count) modulo (block count).

If the multiple command is attempted before the SET MULTIPLE mode command has been executed or when multiple commands are disabled, the multiple operation will be rejected with an Aborted Command Error.

- 56 -

Disk errors encountered during multiple commands will be reported at the beginning of the block or partial block transfer, but DRQ will still be set and the transfer will take place as it normally would, including transfer of corrupt data, if any. Subsequent blocks or partial blocks will only be transferred if the error was a correctable data error. All other errors will cause the command to stop after transfer of the block which contained the error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

### 12.10 Write Multiple Command - C5

The WRITE MULTIPLE command performs similarly to the WRITE SECTORS command except that the controller sets BSY immediately upon receipt of the command, data transfers are multiple sector blocks, and the long bit is not valid. Several sectors are transferred to the Host as a block without intervening interrupts, only requiring DRQ qualification of the transfer at the start of the block, not on each sector. There is no IRQ prior to the first block transfer. The block count, which is the number of sectors to be transferred as block, is programmed by the SET MULTIPLE mode command, which must be executed prior to the WRITE MULTIPLE command. When the WRITE MULTIPLE command is issued, the Sector Count Register will contain the number of sectors (not the number of blocks or the block count) requested. If this sector count is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer will be for N sectors, where N = (sector count) modulo (block count). If the WRITE MULTIPLE command is attempted before the SET MULTIPLE mode command has been executed or when WRITE MULTIPLE commands are disabled, the WRITE MULTIPLE operation will be rejected with an Aborted Command Error.

**Revision B** 

- 57 -

All disk errors encountered during WRITE MULTIPLE commands will be reported after the attempted disk write of the block or partial block is transferred. The write operation will end with the sector in error, even if it was in the middle of a block. Subsequent blocks will not be transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

## 12.11 Set Multiple Mode - C6

This command enables the controller to perform READ MULTIPLE and WRITE MULTIPLE operations and establishes the block count for these commands. Prior to command issuance, the Sector Count Register should be loaded with the number of sectors per block. Block counts supported are multiples of 2 up to the buffer size of each drive, e.g. 1,2,4,8...

Upon receipt of the command, the controller sets BSY and looks at the Sector Count Register contents. If the register contents are valid and a supported block count is supplied, that value is loaded for all subsequent READ **MULTIPLE and WRITE MULTIPLE commands and** execution of these commands is enabled. Any unsupported block count in the register will result in an Aborted Command Error and READ MULTIPLE and WRITE MULTIPLE commands being disabled. If the Sector Count Register contains 0 when the command is issued, READ MULTIPLE and WRITE MULTIPLE commands will be disabled. Once the appropriate action has been taken, the controller resets BSY and generates an interrupt. At power up default is READ MULTIPLE and WRITE MULTIPLE are disabled. The state of READ **MULTIPLE and WRITE MULTIPLE is maintained** through both hardware and software resets.

- 58 -

# 12.12 Power Commands - EX

Commands EO through E3 and E5-E6 constitute the POWER commands. The following table describes these commands:

# **Command** Drive Action

EO	The drive enters STANDBY MODE immediately.
E1	The drive enters IDLE MODE immediately.
E2	The drive enters STANDBY MODE immediately. If the Sector Count register is non-zero then the Auto Power-Down feature is enabled and will take effect when the drive returns to IDLE MODE. If the Sector Count register is zero then the Auto Power-Down feature is disabled.
E3	The drive enters the IDLE MODE immediately. If Sector Count register is non-zero then the Auto Power- Down feature is enabled and will take effect immediately. If the Sector Count register is zero, then the Auto Power- Down feature is disabled.
E5	Puts FF <sub>H</sub> in Sector Count register if drive is in the IDLE MODE. Puts 00 <sub>H</sub> in Sector Count register if drive is in, going to, or recovering from the STANDBY MODE. Puts a BB <sub>H</sub> in the sector count register if power lock is enabled.

**Revision B** 

- 59 -

# E6 The drive enters the SLEEP MODE. A reset is required to bring the drive out of sleep mode.

*Note: Minimum power off/on cycle time should be no less than 3 seconds.* 

All of the POWER commands except command E6 will execute immediately and return the ending interrupt after the spin up/down sequence is initiated. Please note that if the drive is already spinning (IDLE MODE) and a spin up command is issued from the host, the spin up sequence is not initiated.

Similarly, if the drive is in the STANDBY MODE and the host issues a spin down command, the spin down sequence is not initiated. Return of the ending interrupt does not mean that the drive has fully transitioned to the desired operating mode. The SLEEP command is the exception. In command E6, the drive is spun down and when it is stopped, the drive returns the ending interrupt and the SLEEP MODE begins.

When enabling the Auto Power-down feature, the value in the Sector Count Register specifies the number of 5 second increments for the time-out value. If the drive does not receive a command within the specified time, the drive will enter the STANDBY MODE. The minimum time-out value is 60 seconds which means the smallest value for the Sector Count Register is 12 when enabling the Auto Power-down feature. If a number between 1 and 11 inclusive is specified in the Sector Count Register, a value of 12 is used. This prevents overheating of the drive during spin up/down sequences.

- 60 -

The maximum allowable time-out value is 1000 seconds, or 16.6 minutes, resulting in a maximum Sector Count Register value of 200. If a number greater than 200 is specified, a value of 200 is used.

Assertion of Host Reset will only affect the current state of the SLEEP MODE. If the drive is in SLEEP MODE and Host Reset is asserted, the drive wakes up into STANDBY MODE. Please note that the drive will not return to the state it was in when the host issued the sleep command. The default power-on condition of the drive is IDLE MODE.

**Revision B** 

- 61 -

## 12.13 Read Buffer - E4

The READ BUFFER command allows the Host to read the current contents of the drive's sector buffer. Only the Command Register is valid for this command. When this command is issued, the drive will set BSY, set up the sector buffer for a operation, set DRQ, reset BSY, and generate an interrupt. The Host may then read up to 512 bytes of data from the buffer. If 599A<sub>H</sub> is placed in the Cylinder Register then the Sector Count Register is used to pass that many sectors out of the buffer. If the requested sector count is larger than the buffer an Aborted Command error status is returned.

## 12.14 Write Buffer - E8

The WRITE BUFFER command allows the Host to overwrite the contents of the drive's sector buffer with any data pattern desired. Only the Command Register is valid for this command. When this command is issued, the drive will set BSY, set up the sector buffer for a write operation set DRQ, reset BSY. The Host may then write up to 512 bytes of data to the buffer. If  $599A_H$  is placed in the Cylinder Register the Sector Count Register is used to determine how many sectors will be written. If the Sector Count is larger than the buffer an Aborted Command error status is returned.

- 62 -

# 12.15 Identify Drive - EC

The IDENTIFY command allows the Host to receive parameter information from the drive. When the command is issued, the drive sets BSY, stores the required parameter information in the sector buffer, sets the DRQ bit, and generates an interrupt. The Host may then read the information out of the sector buffer. The parameter words in the buffer are arranged as follows, all reserved bits or words should be zeroes. All numbers are given in hexadecimal format right justified. All reserved words are zero.

- Word 00 A constant 0C5A
- Word 01 Default logical cyl.
- Word 02 Number of removable cyl.
- Word 03 Default logical head
- Word 04 Number of unformatted bytes/physical track
- Word 05 Number of unformatted bytes/sector
- Word 06 Default logical sector
- Word 07 Number of bytes in the inter-sector gaps
- Word 08 Number of bytes in the sync fields
- Word 09 0000
- Word 10-19 Serial number
- Word 20 Controller type 0003 dual ported multiple sector buffer with LOOK AHEAD's.
- Word 21 Controller buffer size in 512 byte increments
- Word 22 Number of ECC bytes passed on read/write long commands
- Word 23-26 Controller firmware revision
- Word 27-46 Model number
- Word 47 Number of sectors/interrupt
- Word 48 Double word transfer flag (0 = not capable, 1 = capable)
- Word 49 Assign Alternate (0 = not capable, 1 = capable, See Format Description)
- Word 50 Modes supported (7 XT & AT supported)

**Revision B** 

- 63 -

Word 51 Features supported

Word 52-127 Reserved

Word 128 Native number of cylinders

Word 129 Native number of heads, sectors

Word 130 Current logical number of cylinders

Word 131 Current logical number of heads, sectors

Word 132 Interface flag, Drive Feature bytes.

- bit F Reserved
- bit E Reserved
- bit D Reserved
- bit C Reserved
- bit B Reserved
- bit A Reserved
- bit 9 Reserved
- bit 8 ATA master/slave enable
- bit 7 Enable spindle sync
- bit 6 Reserved
- bit 5 Inhibit spin on power up
- bit 4 Reserved
- bit 3 Disable lookahead read control
- bit 2 Reserved
- bit 1
- bit 0 C flag
- Word 133 Power feature not supported
- Word 134 Identify command flag

bit 15

- thru 2 Undefined
- bit 1 Cam compliant
- bit 0 Physical parameter pointer
  - 0 Physical in words 1,3,6
    - 1 Physical in words 128, 129
- Word 135
- Word 136-255
- Drive Age Reserved

- 64 -

# 12.16 Set Look Ahead Read - EF

This command provides capability to enable or disable the LOOK AHEAD capability. "AA<sub>H</sub>" in the Write Precomp Register enables LOOK AHEADs. The default state on power up or reset is LOOK AHEAD enabled. " $55_{H}$ " disables LOOK AHEADs. Any other values in the Write Precomp Register will result in an Aborted Command Error.

## 12.17 Translate Command - F1

The command uses parameters passed to the drive in the Cylinder High, Cylinder Low, SDH and Sector Number Registers. These values are then translated into the physical location on the drive and values are passed back through their respective registers and a interrupt is sent. An  $AA_H$  must be loaded in the write precomp Register or an Aborted Command error will result.

**Revision B** 

- 65 -

#### 12.18 Physical Seek - F2

The command uses parameters passed to the drive in the Cylinder High, Cylinder Low, and SDH Registers. The parameters are checked for validity and if correct a SEEK is performed to that physical location on the drive. An interrupt will be sent at the start of the SEEK and busy cleared. When the SEEK is complete the SEEK COMPLETE (DSC) bit in the Status Register will be set. Valid cylinder parameters will be 5 to max cylinder (from ID command word 128) if the Sector Count Register contains any value other than FF<sub>H</sub>. If the Sector Count Register contains FF<sub>H</sub> then an offset of 8 will be added to the value in the Cylinder registers. Valid head parameter will be from 0 to max head - 1 (from ID command, word 129, most significant byte). An AA<sub>H</sub> must be loaded in the Precomp Register or an Aborted Command error will result.

- 66 -

## 12.19 Defect List - F5

The command returns three Factory Defect Lists in 6 blocks, the first 4 blocks being the skip list and the last 2 blocks being the alternate list. The drive will set the Sector Count Register to 6 at the start of the command and is the only Register altered as the data is read. Defect information is returned with a 4 byte header followed by 7 byte defect descriptors. The format of the Data is as follows:

Byte 0	-	error log #
Byte 1	-	error log type 0 or 2
Byte 2,3	-	reserved

Seven byte defect descriptors follow in the following format:

Byte 0	-	Error Code
Byte 1	-	Cylinder High
Byte 2	-	Cylinder Low
Byte 3	-	Head
Byte 4	-	Sector
Byte 5	-	Sense
Byte 6	-	Count
0		

**Revision B** 

- 67 -

Each of the logs are 2 blocks long. The error logs will be  $2A_H$  and  $2B_H$  for skip logs and  $2C_H$  for alternate logs. The error code is  $50_H$  for the skip list and  $51_H$  for the alternate list. An AA<sub>H</sub> must be loaded in the Precomp Register or an Aborted Command error will result.

If the precomp Register is loaded with a  $BB_H$  then a scan ID will be performed. The drive will take the physical, not logical, parameters from the Cylinder High, Cylinder Low and drive head Registers and scan that track's ID for alternates. The results will be returned in two 512 byte blocks in the same format as used for the factory defect list.

- 68 -

# 12.20 Enable Index - F6

This command enables an index pulse to be generated by the drive. This pulse is located physically in the same spot across the entire disk. This command will degrade performance of the drive so it should only be used for diagnostic purposes. An AA<sub>H</sub> must be loaded in the Precomp Register or an Aborted Command error will result.

Revision B

- 69 -

# **13.0 Error Reporting**

In general, errors are detected in the following fashion by the drive microprocessor. At the start of the execution of the command, the command register is checked for conditions that would lead to an aborted command. Then the operation is attempted. The errors that are valid for each command are summarized below. Any subsequent error terminates the command at the point that it is discovered.

Command	Error Type Valid
Recalibrate	ABRT, TKO, DRDY, DWF, DSC, ERR
Read Sector(s)	BBK, UNC, IDNF, ABRT, DRDY, DWF, DSC, CORR, ERR
Read Long	BBK, IDNF, ABRT, DRDY, DWF, DSC, ERR
Write Sector(s)	BBK, IDNF, ABRT, DRDY, DWF, DSC, ERR
Write Long	BBK, IDNF, ABRT, DRDY, DWF, DSC, ERR
Verify Sectors	BBK, UNC, IDNF, ABRT, DRDY, DWF, DSC, CORR, ERR
Format Track	IDNF, ABRT, DRDY, DWF, DSC, ERR
Seek	IDNF, ABRT, DRDY, DWF, DSC, ERR
Execute Drive Diag.	ABRT, ERR <sup>1</sup>
Init Driv Parm	ABRT, ERR

- 70 -

Read Multiple	BBK, UNC, IDNF, ABRT, DRDY, DWF, DSC, CORR, ERR
Write Multiple	BBK, IDNF, ABRT, DRDY, DWF, DSC, ERR
Set Multiple	ABRT, ERR
Read Buffer	ABRT, ERR
Write Buffer	ABRT, ERR
Identify Drive	ABRT, ERR
Set Look Ahead Read	ABRT, ERR
Translate Command	ABRT, ERR
Physical Seek	ABRT, ERR
Defect List	ABRT, ERR
Invalid Command Code	ABRT, ERR

1 See Command Description for error byte decoding.

**Revision B** 

- 71 -

# **14.0 Miscellaneous Topics**

The following paragraphs describe operations that span several commands or are not covered sufficiently in the preceding paragraphs.

### 14.1 Reset

A RESET condition will set the DRIVE BUSY, allowing the drive to perform the proper initialization required for normal operation. A RESET condition can be generated in three ways. There are two hardware resets, one from the Host (- HOST RESET) and one from the drive power sense circuitry. These are set 'high' when the system and the drive respectively acknowledge stable power. The other reset is software generated. The Host can write to the Digital Output Register and set the -HOST RESET bit. The Host SOFTWARE RESET condition will persist until the RESET Bit is set to a zero.

Once the RESET has been removed and the drive has been re-enabled, with BSY still active, the drive will perform any necessary hardware initialization, clear any previously programmed drive parameters, revert to the defaults, load the Task File Registers with their initial values, and then reset BSY. No interrupt is generated when initialization is complete. The initial values (hex) for the Task File Registers are as follows:

Error Register	01
Sector Count	01
Sector Number	01
Cylinder Low	00
Cylinder High	00
Drive/Head	00

- 72 -

The drive disables the cache and reallocates the cache to the default number of segments.

## 14.2 Reset Timing

There are two reset conditions: 1) When power is applied and 2) When a SOFTWARE or HARDWARE RESET is received from the host.

When the power is applied to the drive, it performs initialization, executes a ROM test, a buffer memory test, an internal and external RAM test, and then the drive begins spinning up. While the drive is spinning up, the interface is initialized. After going through initialization, the drive waits for the spin up process to complete before setting READY and SEEK COMPLETE in the Status Register and going NOT BUSY. If the drive has previously been commanded to spin down or if it has spun down due to a power command timeout, the drive will not wait for spin up to complete before going NOT BUSY with **READY and SEEK COMPLETE set in the Status** Register. If the drive times out waiting for spin up to complete, it will go NOT BUSY without setting READY and SEEK COMPLETE. When and if the drive completes spin up after timing out, READY and SEEK COMPLETE will be set. The internal timeout for the drive going **READY** is approximately 10 seconds.

When a Host HARDWARE or SOFTWARE RESET is received, only the interface initialization process is executed as previously described.

NOT BUSY. If just a Host HARDWARE or SOFTWARE RESET takes place and the drive is spinning, the reset will only take about 4-6 milliseconds to achieve READY, SEEK COMPLETE and NOT BUSY.

**Revision B** 

- 73 -

## **14.3 Busy Condition**

The status bit for BUSY is set in a number of ways. A RESET condition described previously is one way. Another method occurs when the Host issues a command by writing to the command register. The status register is clocked BUSY on the Host write of the Command Register, for any command except a WRITE, FORMAT or WRITE LONG command. The disk controller and microprocessor prepare the data to return to the host and set the drive NOT BUSY to allow the Host access of the data requested.

On a write type command, the command is issued, setting DATA REQUEST but BUSY is not set until the data to be written is put into the RAM buffer. Write type commands include WRITE SECTOR(s), FORMAT, WRITE SECTOR BUFFER and WRITE LONG.

In addition, the drive microprocessor has the ability to set/reset BUSY. This is the only method that BUSY can be cleared. This means that the only way a drive can respond properly to a command is for the drive microprocessor to be active. When BUSY is active, the drive has read and write access to the Task File Registers and the Host can only read the Status Register and Alternate Status Register of the Task File. Any attempted Host read of a Task File Register, results in reading the Status Register.

When BUSY is inactive, the Host has read and write access to all Task File Registers.

- 74 -

# 14.4 Conner Master/Slave

The drive is equipped with a -C/D jumper. To select the drive as the master, in a two drive or ported system, or a single drive, the -C/D jumper should be installed. If the jumper is not installed, the drive will configure as the slave. The -PDIAG line is used as the slave present signal to the master in the following way.

At power on time -PDIAG will be activated by the slave within 1 ms. If the master does not see -PDIAG active after 4 ms it will assume no slave is present. -PDIAG will remain active until the slave is ready to go not busy or 14.0 seconds after a Power On Reset. The master will wait 14.5 seconds or until the slave deactivates -PDIAG on Power On Reset before it goes not busy. The slave will deactivate -PDIAG and go not busy, if it is not ready after the 14.0 seconds. Neither drive will set Ready or Seek Complete until they have reached full spin speed and are ready to read and write.

During a software reset, -PDIAG will be activated by the slave within 1 millisecond. If the master does not see -PDIAG active after 4 ms it will assume that no slave is present. The slave will not deactivate -PDIAG until it is ready to go not busy or 400 ms. The master will only wait 450 ms or until the slave deactivates -PDIAG before it goes not busy. The slave will only wait 450 ms before it activates -PDIAG and goes not busy. The drive will not set Ready or Seek Complete until those states are achieved.

After Reset, -PDIAG is used in its normal diagnostic function during the diagnostic command.

**Revision B** 

- 75 -

## 14.5 Error Detection and Correction (EDAC)

The drive uses a Reed-Solomon code to perform error detection and correction. The polynomial is able to detect a single burst of up to 51 bits in length or up to three bursts each of which may be up to 11 bits in length.

The error correction capability of the polynomial is a single error burst with a maximum length of 22 bits or two independent error bursts of up to 11 bits each per 512 byte block. A single burst of 11 bits or less is corrected "on-the-fly" with no performance degradation. The miscorrection probability using this "on-the-fly" error correction is superior to the detection capability of the traditionally used 56 bit computer generated code.

- 76 -